

WHAT IS CLAIMED IS:

Claim 1:

1 1. A circuit apparatus associated with a mid-level cache for handling side-door
2 communal software lock (CSWL) inquiries in a multiple instruction-processor computer
3 system comprising:
4 a. inquiry generator for generating signals containing either CSWL requests
5 or status reports regarding locked status of a CSWL and for providing such
6 inquiries and reports to another mid-level cache side door,
7 b. receiving circuit for receiving said CSWL inquiries and reports,
8 c. Interpreter for reading the signals in said CSWL inquiry to determine if it
9 relates to a CSWL mapped to said associated mid-level cache and what each
10 particular lock request function requires for any of said CSWL requests,
11 d. CSWL cache memory within said associated mid-level cache for storing
12 CSWLs to which said associated mid-level cache is mapped, and means for
13 determining if a CSWL which is subject to said CSWL inquiry is present within
14 said CSWL cache memory,
15 e. comparator circuit for determining a current value of a requested CSWL
16 within said mid-level cache's memory,
17 f. CSWL inquiry processor for processing said CSWL inquiry and for
18 generating a response to said CSWL inquiry,
19 g. A circuit for responding to a requesting local processor with the status
20 received from a status report.

Claim 2:

1 2. The circuit apparatus of claim 1 wherein said CSWL inquiry processor is said
2 means for determining of part "d".

Claim 3:

1 3. The circuit apparatus of claim 1 wherein said CSWL inquiry processor includes
2 said comparator circuit.

Claim 4:

1 4. The circuit apparatus of claim 1 further comprising a CSWL map directory for
2 said associated mid-level cache containing addresses for each CSWL to which said
3 associated mid-level cache is mapped and wherein said CSWL inquiry processor further
4 comprises a circuit for determining whether a CSWL inquiry is mapped to said
5 associated mid-level cache.

Claim 5:

1 5. The circuit apparatus of claim 4 further comprising a lock request generator for
2 generating an inter-mid-level cache lock requests to send to other, non-associated mid-
3 level caches if said CSWL inquiry processor determines a CSWL inquiry is not mapped
4 to said associated mid-level cache.

Claim 6:

1 6. The circuit apparatus of claim 4 further comprising a lock request generator for
2 generating an inter-mid-level cache lock requests to send a CSWL lock function to the
3 CSWL data determined to be mapped to another, non-associated mid-level cache if said
4 CSWL inquiry processor determines a CSWL inquiry is not mapped to said associated
5 mid-level cache but is mapped to said non-associated mid-level cache.

Claim 7:

1 7. The circuit apparatus of claim 5 wherein said lock request generator for
2 generating lock requests determines from information in said CSWL map directory which
3 other, non-associated mid-level cache to which to direct said inter-mid-level cache lock
4 request.

Claim 8:

1 8. The circuit apparatus of claim 1 further comprising a status stripper (?) circuit for
2 fashioning a signal from a status field in a CSWL after processing by said CSWL inquiry
3 processor to supply information needed to provide a reply to said CSWL inquiry.

Claim 9:

1 9. The circuit apparatus of claim 1 further comprising a side-door circuit for
2 receiving said CSWL inquiries and status reports from other, non-associated mid-level
3 caches having similar circuit apparatus to said claim 1 circuit apparatus through which to
4 communicate with said other, non-associated mid-level caches said similar circuit
5 apparatuses.

Claim 10:

1 10. The circuit apparatus of claim 8 wherein CSWL inquiries from processor units
2 associated with said associated mid-level cache are received by said circuit apparatus
3 through an internal data channel.

Claim 11:

1 11. The circuit apparatus of claim 1 wherein access to said lock cache is given a
2 lower priority than access to a data cache in said associated mid-level cache.

Claim 12:

1 12. A computer system having a set of mid-level caches connected through said side
2 door to side doors of said similar circuit apparatae in each of said non-associated mid-
3 level caches, and wherein a radial communications pathway joins all such side doors.

Claim 13:

1 13. A computer system as set forth in claim 9 wherein the radial is a bus and the
2 connection is a side door programmed to respond only to mapped CSWLs appearing on
3 the bus.

Claim 14:

1 14. A computer system as set forth in claim 9 wherein the radial is a crossbar and
2 the connections are configured by mapping of said CSWLs such that a given CSWL will
3 map to a unique mid-level cache.

Claim 15:

1 15. A method for handling communal software locks (CSWLs) among a set of
2 controller circuits situated in an associated set of mid-level caches in a multiprocessor
3 computer system, comprising:

4 A) receiving a request for a software lock by a one of said set of controller
5 circuits in a receiving one of said set of controller circuits (a receiving controller)
6 from a requester,

7 B) interpreting said software lock request and if said interpreting yields a
8 determination that said software lock request relates to a CSWL, then:

9 C) determining if said requested CSWL is mapped to said receiving
10 controller and if mapped to said receiving controller:

11 1. searching said associated mid level cache for presence of said
12 CSWL in said associated mid level cache,

13 2. if said requested CSWL is in a storage circuit in said associated
14 mid level cache either:

15 a. setting said requested CSWL and returning an ownership
16 indicia to said requester, or

17 b. if said requested CSWL is owned by another, returning a
18 status to said requester,

19 3. if said requested CSWL is not in a storage circuit within said
20 associated mid level cache:

21 a. forming a data request for the requested CSWL and
22 sending said data request to said multiprocessor computer system
23 to retrieve the requested CSWL from a current owner

24 b. receiving said requested CSWL from said multiprocessor
25 computer system and processing said request in accord with sub-
26 step 2, and

27 D) if said software lock request does not relate to a CSWL, passing said
28 software lock request as ordinary data within said computer system.

Claim 16:

- 1 16. The method of claim 15 wherein step C 2) is performed by said receiving
2 controller in said associated cache and wherein said requested CSWL is retained by
3 said associated mid level cache.

Claim 17:

- 1 17. The method of claim 15 wherein said interpreting of step B comprises;
2 recognizing whether said request has been received into said associated
3 mid level cache through a side door, and if received through said side door then
4 determining that said request is a CSWL request.

Claim 18:

- 1 18. The method of claim 16 wherein said interpreting of step B comprises:
2 setting a flag indicator by a processor which uses said associated mid
3 level cache to indicate that a software lock request is a CSWL request and
4 recognizing said flag indicator by said receiving controller.

Claim 19:

- 1 19. The method of claim 15 further comprising prioritizing step C wherein step C will
2 be performed by said set of mid level caches only after other mid level cache functions.

Claim 20:

- 1 20. The method of claim 15 further comprising prioritizing step C to be performed at
2 a lower priority than other functions of said mid level cache, on an interleaved basis.

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